Standard Products

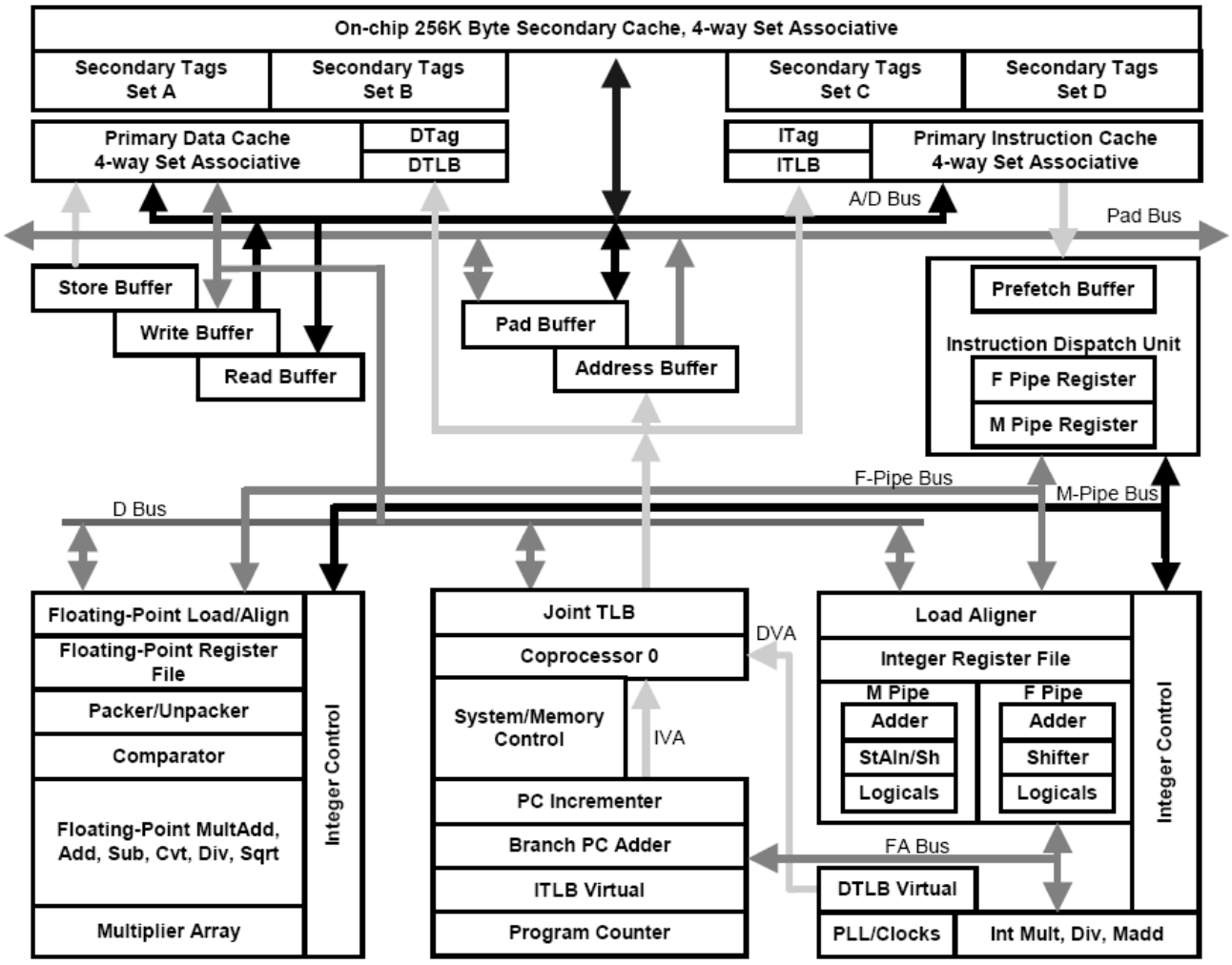
MIP7365
64-Bit Superscaler Microprocessor

February 17, 2012

FEATURES

- Upscreened PMC-Sierra RM7065C
- Military and Industrial Grades Available
- Dual issue symmetric superscalar microprocessor with instruction prefetch optimized for system level price/performance
  - o 450MHz operating frequency
- High-performance system interface
  - o Multiplexed address/data bus (SysAD) supports 2.5V, 3.3V I/O logic
  - o Processor clock multipliers 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9
  - o Support for 64-bit or 32-bit external agents
- Integrated primary and secondary caches
  - o All are 4-way set associative with 32-byte line size
  - o 16-Kbytes instruction, 16-Kbytes data, 256-Kbytes on-chip secondary
  - o Per line cache locking in primaries and secondary
  - o Fast Packet Cache™ increases system efficiency in networking applications
- High-performance floating-point unit — 1600MFLOPS maximum
  - o Single cycle repeat rate for common single-precision operations and some double-precision operations
  - o Single cycle repeat rate for single-precision combined multiply-add operations
  - o Two cycle repeat rate for double-precision multiply and double-precision combined multiply-add operations
- MIPS IV superset instruction set architecture
  - o Data PREFETCH instruction allows the processor to overlap cache miss latency and instruction execution
  - o Single-cycle floating-point multiply-add
- Integrated memory management unit
  - o Fully associative joint TLB (shared by I and D translations)
  - o 64/48 dual entries map 128/96 pages
  - o Variable page size
- Embedded application enhancements
  - o Specialized DSP integer Multiply-Accumulate instructions, (MAD/MADU) and three-operand multiply instruction (MUL)
  - o I&D Test/Break-point (Watch) registers for emulation & debug
  - o Performance counter for system and software tuning & debug
  - o Fourteen fully prioritized vectored interrupts — 10 external, 2 internal, 2 software
- Fully static CMOS design with dynamic power down logic
- 216-EPad LQFP 24x24mm are pin compatible with the RM7965 and RM5261A EPad™ products

NOTE: 216-Enhanced Pad package, EPad MIPS64 and Fast Packet Cache are Trademarks of PMC-Sierra



BLOCK DIAGRAM

DESCRIPTION

The MIP7365 Microprocessor is a highly integrated symmetric superscalar microprocessor capable of issuing two instructions each processor cycle. It has two high performance 64-bit integer units as well as a high-throughput, fully pipelined 64-bit floating point unit.

The MIP7365 integrates 16 Kbytes 4-way set associative instruction and data caches along with an integrated 256 Kbytes 4-way set associative secondary cache. The primary data and secondary caches are write-back and non-blocking.

The memory management unit contains a 64/48-entry fully associative TLB and a 64-bit system interface supporting multiple outstanding reads with out-of-order return and hardware prioritized and vectored interrupts.

The MIP7365 is available in a 216-EPad LQFP package and a 256-pin TBGA package. The 216-EPad package is pin compatible with previous RM7965 and the RM5261A ExposedPad products.

The MIP7365 ideally suits high-end embedded control applications such as internetworking, high-performance image manipulation, high-speed printing, and 3-D visualization. The MIP7365 is also applicable to the low end workstation market where its balanced integer and floating-point performance provides outstanding price/performance.

For additional Detail Information regarding the operation of the PMC-Sierra see the latest PMC-Sierra datasheet for the RM7065C Family Microprocessors Data Sheet, Issue No. 5: August 2006; Document No. PMC-2021816, Issue 5

PIN DESCRIPTIONS

The following is a list of control, data, clock, interrupt, and miscellaneous pins of MIP7365.

System Interface

PIN NAME	TYPE	DESCRIPTION
ExtRqst*	Input	External request Signals that the external agent is submitting an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
PRqst*	Output	Processor Request When asserted this signal requests that control of the system interface be returned to the processor. This is enabled by Mode Bit 26
PAck*	Input	Processor Acknowledge When asserted, in response to PRqst*, this signal indicates to the processor that it has been granted control of the system interface.
RspSwap*	Input	Response Swap RspSwap* is used by the external agent to signal the processor when it is about to return a memory reference out of order; i.e., of two outstanding memory references, the data for the second reference is being returned ahead of the data for the first reference. In order that the processor will have time to switch the address to the tertiary cache, this signal must be asserted a minimum of two cycles prior to the data itself being presented. Note that this signal works as a toggle; i.e., for each cycle that it is held asserted the order of return is reversed. By default, anytime the processor issues a second read it is assumed that the reads will be returned in order; i.e., no action is required if the reads are indeed returned in order. This is enabled by Mode Bit 26.
RdType	Output	Read Type During the address cycle of a read request, RdType indicates whether the read request is an instruction read or a data read.
SysAD[63:0]	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC[7:0]	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmd[8:0]	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System Command/Data Identifier Bus Parity For the MIP7365, unused on input and zero on output.

Clock/Control Interface

PIN NAME	TYPE	DESCRIPTION
SysClock	Input	System clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
SysClock*	Input	System clock Differential clock input used only in HSTL I/O mode. Set SysClock* to VccIO or Do Not Connect for non-HSTL operation.

Power Supply

PIN NAME	TYPE	DESCRIPTION
VccInt	Input	Power supply for core.
VccIO	Input	Power supply for I/O.
VccP	Input	Vcc for PLL Quiet VccInt for the internal phase locked loop. Must be connected to VccInt through a filter circuit.
VccJ	Input	Power supply used for JTAG.
VREF_In	Input	Reference voltage for HSTL I/O. Do not connect for non-HSTL.
Vss	Input	Ground Return.
VssP	Input	Vss for PLL Quiet Vss for the internal phase locked loop. Must be connected to Vss through a filter circuit.

Interrupt Interface

PIN NAME	TYPE	DESCRIPTION
INT[9:0]*	Input	Interrupt Ten general processor interrupts, bit-wise ORed with bits 9:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 15 of the interrupt register (bit 6 in R5000 compatibility mode).

JTAG Interface

PIN NAME	TYPE	DESCRIPTION
JTDI	Input	JTAG data in
JTCK	Input	JTAG clock input
JTDO	Output	JTAG data out
JTMS	Input	JTAG command
JTRST*	Input	JTAG reset.

Notes:
1. The **JTRST*** input was added to the RM70xxC and RM79xx CPUs to directly control the reset to the JTAG state machine. JTAG boundary scan test equipment must be able to drive **JTRST*** high to allow JTAG boundary scan operation.
2. The **JTRST*** input must be connected to GND (**Vss**) through a 220Ω to 1 KΩ pull-down resistor to force the JTAG state machine into the reset state to allow normal operation (JTAG boundary scan mode disabled).
3. The JTAG interface electrical characteristics are dependent on the **VccJ** level chosen (2.5 V or 3.3 V).

Initialization Interface

PIN NAME	TYPE	DESCRIPTION
BigEndian	Input	Big Endian / Little Endian Control Allows the system to change the processor addressing
VccOK	Input	Vcc is OK When asserted, this signal indicates to the MIP7365 that the VccInt power supply has been above the recommended value for more than 100 milliseconds and will remain stable. The assertion of VccOK initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold Reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with SysClock.
ModeClock	Output	Boot Mode Clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
Modein	Input	Boot Mode Data In Serial boot-mode data input.
HSTL-Sel*	Input	HSTL/VTL Control Asserting this signal low places the system I/O pins in HSTL mode. Pulling this signal high or allowing to float places all system I/O pins in LVTLL mode.

Notes:
1. In HSTL mode, maximum voltage level of ModeClock is determined by VccJ level.
2. SysClock*, VREF_In, and HSTL-SEL* signal pin are no connect on LVTTL mode.
3. Functionality of the HSTL mode is not tested by Aeroflex and guaranteed to work at Industrial temperatures only.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	RANGE	UNITS
V_{TERM}	Terminal Voltage with respect to Vss	-0.5[2] to 3.9	V
Tc	Operating Temperature I = Industrial R = Extended T = Military M = Military, Screened	 -40 to +85 -55 to +110 -55 to +125 -55 to +125	 •C •C •C •C
T_{STG}	Storage Temperature	-55 to +125	•C
I_{IN}	DC Input Current	±20	mA
I_{OUT}	DC Output Current [4]	±20	mA

Notes:

1. Stresses above those listed under "*Absolute Maximums Rating*" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VIN minimum = -2.0V for pulse width less than 15nS. VIN maximum should not exceed +3.95 Volts.
3. When VIN < 0V or VIN > VccIO.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

RECOMMENDED OPERATING CONDITIONS

GRADE	CPU SPEED	TEMP (CASE)	Vss	VccInt	VccIO	VccP	VccJ
Industrial	450 MHz	-40°C to +85°C	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6
Extended	450 MHz	-55°C to +110°C	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6
Military	450 MHz	-55°C to +125°C Note 5	0 V	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6	1.3 V ± 50 mV	3.3 V ± 150 mV or 2.5 V ± 200 mV Note 6

Notes

1. VccIO should not exceed VccInt by greater than 2.5 V during the power-up sequence.
2. Applying a logic high state to any I/O pin before VccInt becomes stable is not recommended.
3. As specified in IEEE 1149.1 (JTAG), the JTMS pin must be held high during reset to avoid entering JTAG test mode. Refer to the RM7000 User Manual.
4. VccP must be connected to VccInt through a passive filter circuit. See RM7000 User Manual fo recommended circuit.
5. Contact factory for extended military temperature range products (CQFP hermetic MCM packages will be screened at -55°C to + 125°C).
6. These voltages are recommended for HSTL mode operations only. HSTL mode operation is guaranteed at Industrial temperatures only.

DC ELECTRICAL CHARACTERISTICS

VccIO = 3.15 - 3.45V

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{OL}	-	0.2V	$\|I_{OUT}\|$ = 100µA
V_{OH}	VccIO - 0.2V	-	
V_{OL}	-	0.4V	$\|I_{OUT}\|$ = 2mA
V_{OH}	2.4V	-	
V_{IL}	-0.3V	0.8V	-
V_{IH}	2.0V	VccIO + 0.3V	-
I_{IN}	- -	±5µA ±5µA	V_{IN} = 0 V_{IN} = VccIO

VccIO = 2.3V – 2.7V

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{OL}	-	0.2V	$\|I_{OUT}\|$ = 100µA
V_{OH}	2.1V	-	
V_{OL}	-	0.4V	$\|I_{OUT}\|$ = 1mA
V_{OH}	2.0V	-	
V_{OL}	-	0.7V	$\|I_{OUT}\|$ = 2mA
V_{OH}	1.7V	-	
V_{IL}	-0.3V	0.7V	-
V_{IH}	1.7V	VccIO + 0.3V	-
I_{IN}	- -	±15µA ±15µA	V_{IN} = 0 V_{IN} = VccIO

POWER CONSUMPTION

PARAMETER		CONDITIONS	CPU SPEED	
			450MHz (IND)	450MHz (MIL)
			MAX	MAX
V_{CCINT} Power (mWatts)	Standby		1350	1350
	Active	Maximum with no FPU operation [2]	3100	3250
		Maximum worst case instruction mix	3250	3400

Notes:
1. Worst case supply voltage (maximum VccInt) with worst case temperature (maximum T_{CASE}).
2. Dhrystone 2.1 instruction mix.
3. I/O supply power is application dependant, but typically <20% of VccInt.

AC CHARACTERISTICS

CAPACITIVE LOAD DERATION

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS	Mode
C_{LD}	Load Derate	-	2	ns/25pF	LVTTL

CLOCK PARAMETERS

PARAMETER	SYMBOL	TEST CONDITIONS	BUS SPEED		UNITS
			LVTTL		
			MIN	MAX	
SysClock High	t_{SCHigh}	Transition ≤ 2ns	3	-	ns
SysClock Low	t_{SCLow}	Transition ≤ 2ns	3	-	ns
SysClock Frequency[1]			33.3	133	MHz
SysClock Period	t_{SCP}		7.5	30	ns
Clock Jitter for SysClock	$t_{JitterIn}$		-	±150	ps
SysClock Rise Time	t_{SCRise}		-	2	ns
SysClock Fall Time	t_{SCFall}		-	2	ns
ModeClock Period	$t_{ModeCKP}$		-	256	ns
JTAG Clock Period	$t_{JTAGCKP}$		4	-	ns

Notes:
1. Operation of the MIP7365 is only guaranteed with the Phase Loop enabled.

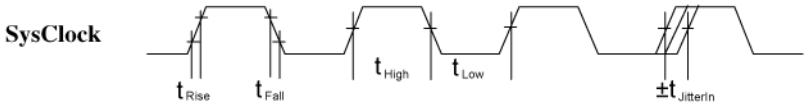
SYSTEM INTERFACE PARAMETERS

PARAMETER[1]	SYM	TEST CONDITIONS[5,6]	I/O TYPE		UNITS
			LVTTL I/O		
			MIN	MAX	
Data Output[2,6,7]	t_{DO}	LVTTL (VccIO = 3.3V): mode[14:13] = 10 (fastest)	0.75	4.5	ns
		LVTTL (VccIO = 3.3V): mode[14:13] = 01 (slowest)	0.75	5.5	ns
Data Setup[4]	t_{DS}	t_{RISE} = See above table	2.5	-	ns
Data Hold[4]	t_{DH}	t_{FALL}= See above table	1.0	-	ns

Notes
1. In LVTTL mode, timings are measured from 0.425 x **VccIO** of clock to 0.425 x **VccIO** of signal for 3.3V I/O, and from 0.48 x **VccIO** of clock to 0.48 x **VccIO** of signal for 2.5V I/O. Input Rise/Fall time = 1V/1ns.
2. Capacitive load for all LVTTL maximum output timings is 50 pF. Minimum output timings are for theoretical no load conditions - untested.
4. Data Output timing applies to all signal pins whether tristate I/O or output only.
5. Setup and Hold parameters apply to all signal pins whether tristate I/O or input only.
6. Only mode 14:13 = 01 is tested and guaranteed.
7. Data shown is for 3.3 V I/O. For 2.5 V I/O: derate t_{DO} min by 0.25 nS, and t_{DO} max by 0.5 nS. Mode setting is mode [14:13] = 10 (fastest) or 01 (slowest).

TIMING DIAGRAMS

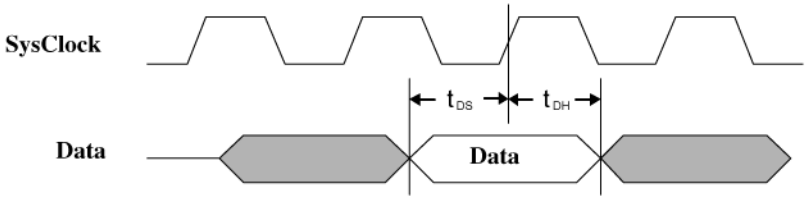
CLOCK TIMING



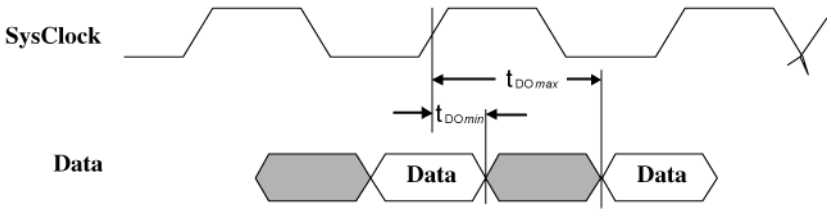
SYSTEM INTERFACE TIMING

(SysAD, SysCmd, ValidIn*, ValidOut*, etc.)

INPUT TIMING



OUTPUT TIMING

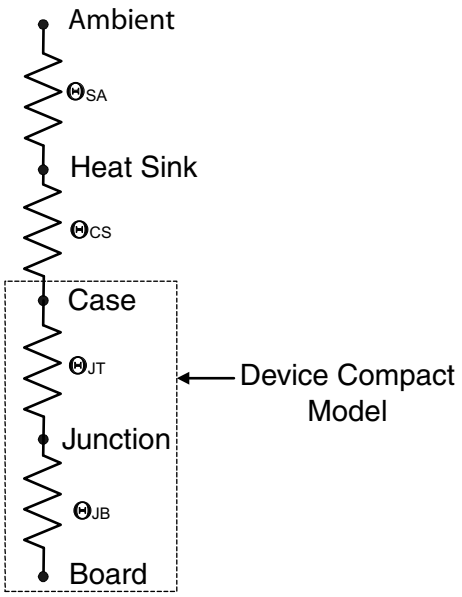


THERMAL INFORMATION

This product is designed to operate over a wide temperature range when used with a heat sink.

Maximum long-term operating junction temperature to ensure adequate long-term life	TBD at 450 MHz
Maximum junction temperature for short-term excursions with guaranteed continued functional performance	TBD at 450 MHz
Minimum ambient temperature	TBD

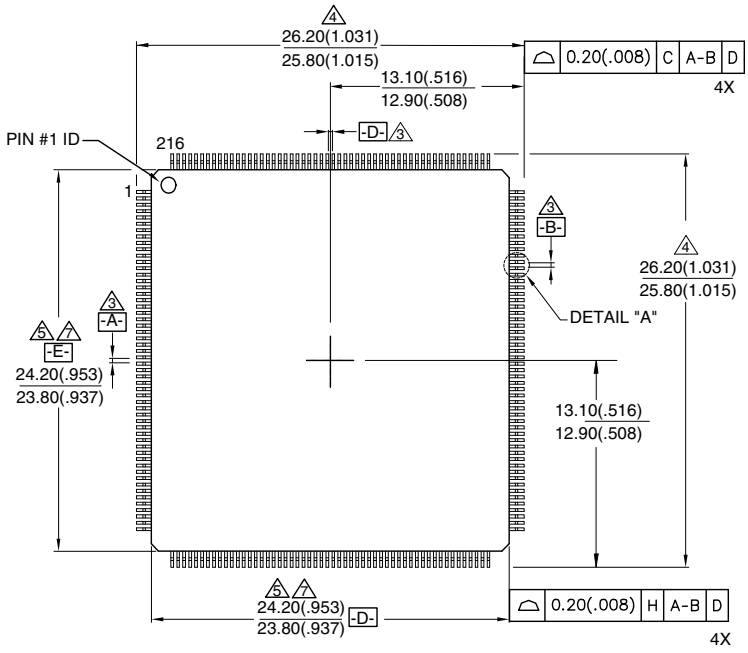
Device Compact Model [2]	
θ_{JT} (°C/W)	4.19
θ_{JB} (°C/W)	5.43
θ_{JA} (°C/W)	11.65



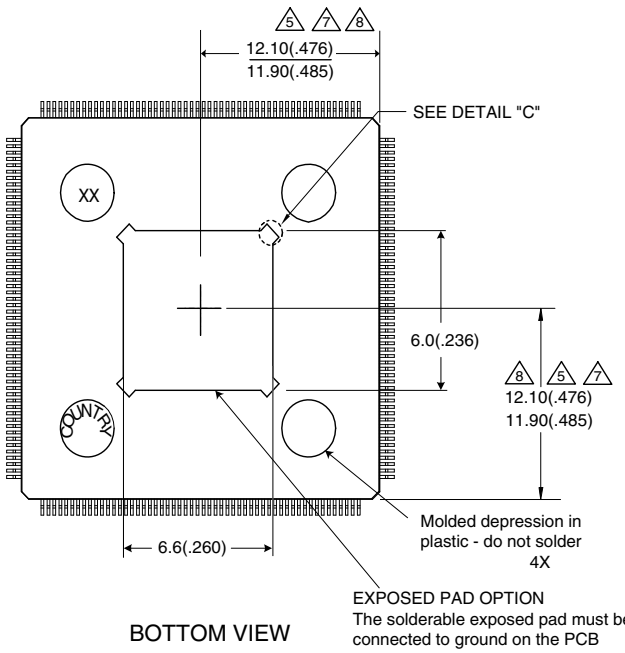
Operating power is dissipated in any package (watts) offered at worst case power supply		
Power at 450MHz	VccInt = 1.3 V, VccIO = 3.3 V	2.8W

Notes
1. Short-term is understood as the definition stated in Telcordia Generic Requirements GR-63-Core.
2. θ_{JC}, the junction-to-case thermal resistance, θ_{JB}, the junction-to-board thermal resistance are obtained from Package vendor.
3. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material.
4. The actual θSA required may vary according to the air speed at the location of the device in the system with all the components in place.

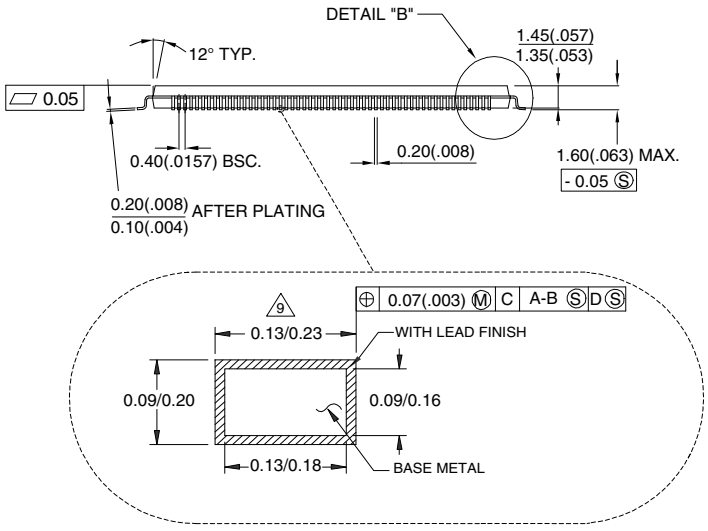
MIP7365 216-PIN EPad LQFP PACKAGE OUTLINE



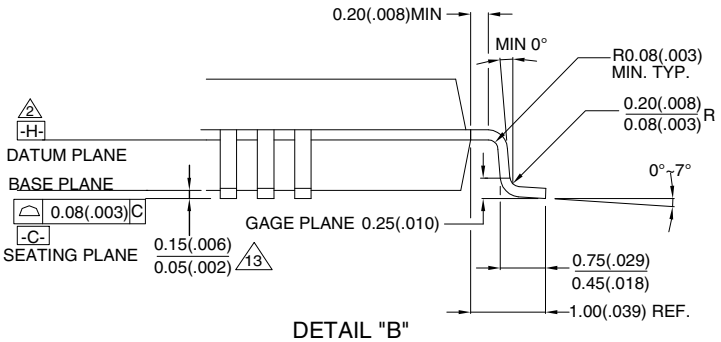
TOP VIEW



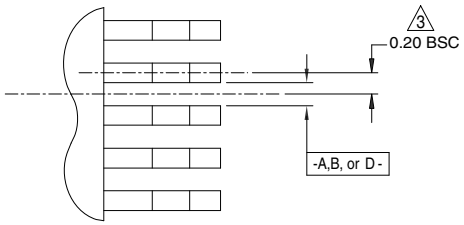
BOTTOM VIEW



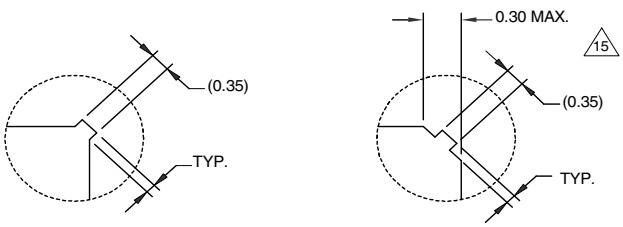
SIDE VIEW



DETAIL "B"



DETAIL "A"



DETAIL "C"
(EXPOSED PAD CORNER DETAIL)

MIP7365 216-PIN EPad LQFP PACKAGE OUTLINE NOTES

Notes

1. All dimensions and tolerancing conform to ANSI Y14.5-1982. Inches are shown in parentheses.

2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.

3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.

4. To be determined at seating plane -C-.

5. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254 mm on dimensions.

6. 216 is the total number of terminals.

7. These dimensions to be determined at datum plane -H-.

8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.

9. Dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.

10. Controlling dimension: millimeter.

11. Maximum allowable die thickness to be assembled in this package family is 0.38 mm.

12. This outline conforms to JEDEC publication 95, registration MS-026, variation BGB.

13. Defined as the distance from the seating plane to the lowest point of the package body.

14. Exposed pad shall be coplanar with bottom of package within 0.05.

15. Corner chamfer of exposed die pad shall be within 0.30 mm.

MIP7365 216-EPad LQFP NUMERICAL PINOUT vs FUNCTION [1,2]

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	VccIO	39	SysAD48	77	VccIO	115	JTDO
2	Do Not Connect	40	SysAD16	78	SysCmd5	116	VccIO
3	Do Not Connect	41	VccInt	79	SysCmd4	117	ModeClock
4	Do Not Connect	42	BigEndian	80	SysCmd3	118	VccInt
5	Do Not Connect	43	VccIO	81	SysCmd2	119	PRQST*
6	VccInt	44	VccOK	82	VccInt	120	PACK*
7	SysAD59	45	ColdReset*	83	SysCmd1	121	RspSwap*
8	SysAD27	46	Reset*	84	SysCmd0	122	VccIO
9	SysAD58	47	ExtRqst*	85	Do Not Connect	123	VccInt
10	VccInt	48	NMI*	86	Do Not Connect	124	SysAD47
11	VccIO	49	VccInt	87	Do Not Connect	125	SysAD15
12	SysAD26	50	INT9*	88	VccInt	126	VccInt
13	VccInt	51	INT8*	89	Do Not Connect	127	SysAD46
14	SysAD57	52	INT7*	90	Do Not Connect	128	SysAD14
15	SysAD25	53	INT6*	91	VccInt	129	SysAD45
16	SysAD56	54	VccIO	92	Do Not Connect	130	SysAD13
17	SysAD24	55	VccJ	93	Do Not Connect	131	SysAD44
18	SysAD55	56	VccIO	94	Do Not Connect	132	SysAD12
19	SysAD23	57	INT5*	95	VccInt	133	VccInt
20	VccInt	58	INT4*	96	Do Not Connect	134	SysAD43
21	SysAD54	59	INT3*	97	Master Clock	135	SysAD11
22	SysAD22	60	INT2*	98	VssP	136	VccIO
23	SysAD53	61	INT1*	99	VccP	137	VccIO
24	SysAD21	62	INT0*	100	Release*	138	SysAD42
25	VccIO	63	VccInt	101	ValidOut*	139	SysAD10
26	VccIO	64	VccInt	102	ValidIn*	140	SysAD41
27	VccIO	65	Do Not Connect	103	WrRdy*	141	SysAD9
28	SysAD52	66	Do Not Connect	104	RdRdy*	142	VccInt
29	SysAD20	67	Do Not Connect	105	Do Not Connect	143	SysAD40
30	VccInt	68	VccIO	106	ModeIn	144	SysAD8
31	SysAD51	69	Do Not Connect	107	RdType	145	SysAD39
32	SysAD19	70	Do Not Connect	108	Do Not Connect	146	SysAD7
33	SysAD50	71	Do Not Connect	109	VccJ	147	SysAD38
34	SysAD18	72	VccInt	110	JTRST*	148	SysAD6
35	SysAD49	73	SysCmdP	111	VccIO	149	VccInt
36	SysAD17	74	SysCmd8	112	JTMS	150	SysAD37
37	VccIO	75	SysCmd7	113	JTCK	151	SysAD5
38	VccInt	76	SysCmd6	114	JTDI	152	SysAD36

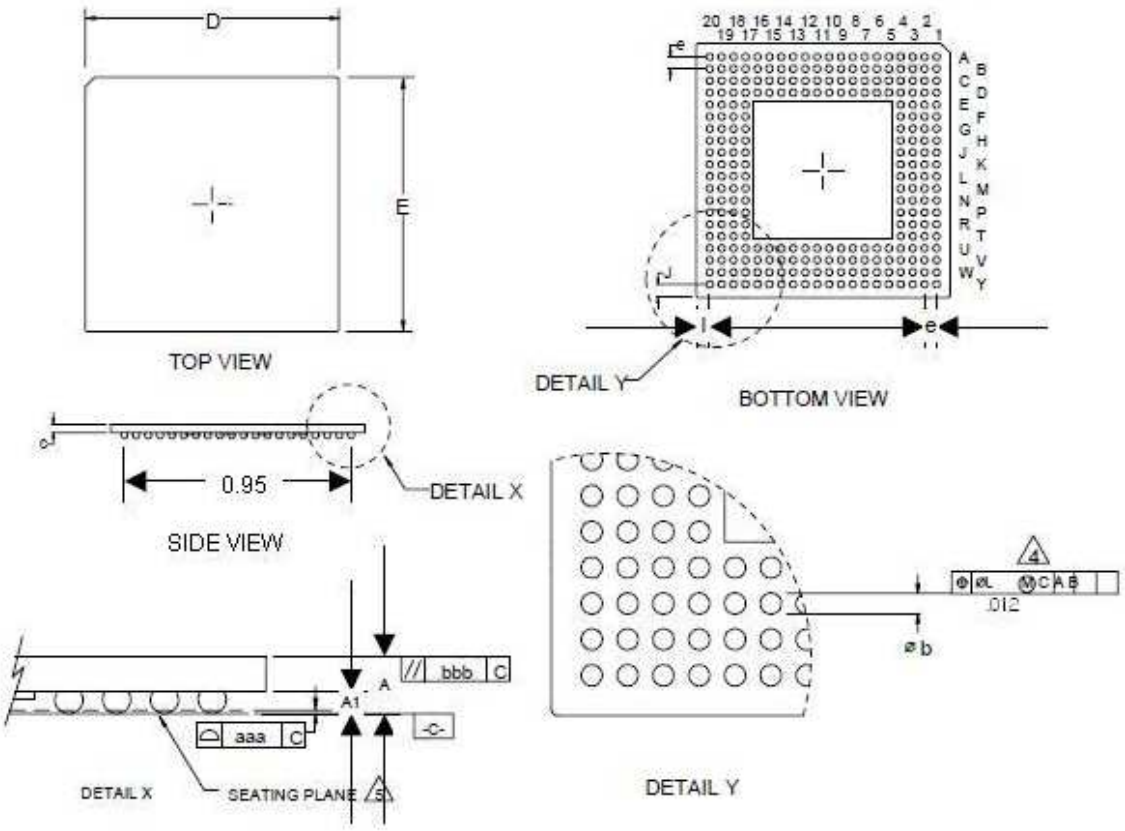
MIP7365 216-EPad LQFP NUMERICAL PINOUT vs FUNCTION [1,2] CON'T

PIN	FUNCTION	PIN	FUNCTION
153	SysAD4	191	VccIO
154	VccInt	192	SysADC7
155	Do Not Connect	193	SysADC3
156	Do Not Connect	194	VccInt
157	VccInt	195	SysADC6
158	Do Not Connect	196	VccIO
159	Do Not Connect	197	SysADC2
160	Do Not Connect	198	SysAD63
161	Do Not Connect	199	SysAD31
162	VccIO	200	Do Not Connect
163	Do Not Connect	201	SysAD62
164	VccIO	202	SysAD30
165	VccIO	203	VccIO
166	Do Not Connect	204	VccIO
167	Do Not Connect	205	VccInt
168	Do Not Connect	206	SysAD61
169	Do Not Connect	207	SysAD29
170	SysAD35	208	VccInt
171	SysAD3	209	SysAD60
172	VccInt	210	SysAD28
173	SysAD34	211	Do Not Connect
174	SysAD2	212	Do Not Connect
175	VccInt	213	Do Not Connect
176	VccIO	214	Do Not Connect
177	VccInt	215	VccIO
178	SysAD33	216	VccIO
179	SysAD1		
180	SysAD32		
181	SysAD0		
182	SysADC5		
183	SysADC1		
184	VccIO		
185	VccInt		
186	SysADC4		
187	SysADC0		
188	Do Not Connect		
189	VccInt		
190	VccIO		

Notes:

1. The exposed pad on the bottom of the EPad LQFP package acts as the sole device ground and as the primary heat conduction path. As such, it must be soldered to the printed circuit board.
2. See PMC-***2030256***, 216-EPad LQFP Design Guidelines Application Note for details.

MIP7365
256 TBGA PACKAGE OUTLINE



Symbol	MIN	NOM	MAX
A8	--	--	.067
A1	.020 (0.50)	.024 (0.60)	.028 (0.70)
D		1.063 (27.00)	
E		1.063 (27.00)	
I	.056 REF (1.435)		
J	.056 REF (1.435)		
M	.787 <PERIMETER> (20)		
aaa			.008 (0.20)
bbb			.010 (0.25)
b	.024 (0.60)	.030 (0.75)	.035 (0.90)
c	.031 (0.80)	.035 (0.90)	.039 (1.00)
e	.050 TYP (1.27)		

MIP7365 256 TBGA PACKAGE OUTLINE NOTES

Notes

1. Package dimensions conform to JEDEC Registration MO-149(BG-2X).
2. "e" represents the basic solder ball grid patch.
3. "M" represents the maximum solder ball matrix size.
4. Dimension "b" is measured at the maximum solder ball diameter parallel to the primary datum "c".
5. The Primary datum "c" and the seating plane are defined by the spherical crowns of the solder balls.
6. All dimensions are in inches.
7. Dimensioning and tolerancing per ASME Y-14.5M-1994.
8. After surface mount assembly solder ball will have 0.006" (TYP) collapse in "A" dimension.
9. Substrate base material is copper.
10. Package top surface shall be black.
11. Cavity depth maximum is .020".

MIP7365 256 TBGA NUMERICAL PINOUT vs FUNCTION [1,2]

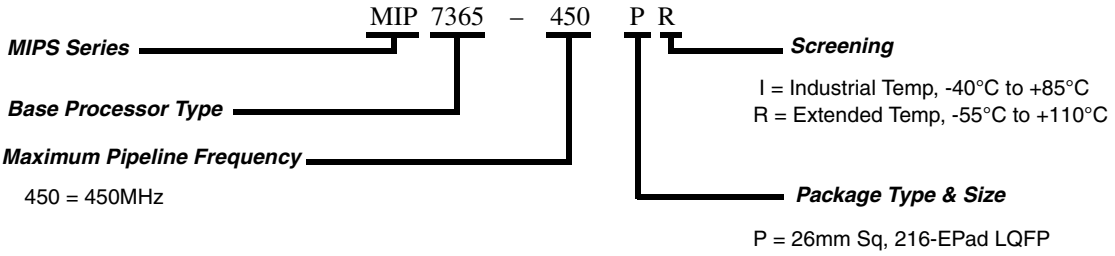
Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VccIO	A2	Vss	A3	Vss	A4	Do Not Connect
A5	SysAD35	A6	Vss	A7	SysAD33	A8	SysAD32
A9	Vss	A10	SysADC1	A11	HSTL_Sel*	A12	Vss
A13	SysADC2	A14	SysAD62	A15	Vss	A16	SysAD60
A17	Do Not Connect	A18	Vss	A19	Vss	A20	VccIO
B1	Vss	B2	VccIO	B3	Vss	B4	Vss
B5	Do Not Connect	B6	SysAD3	B7	SysAD2	B8	SysAD1
B9	SysADC5	B10	SysADC0	B11	SysADC3	B12	SysADC6
B13	VREF-In	B14	SysAD30	B15	SysAD29	B16	Do Not Connect
B17	Vss	B18	Vss	B19	VccIO	B20	Vss
C1	Vss	C2	Vss	C3	VccIO	C4	Do Not Connect
C5	Do Not Connect	C6	Do Not Connect	C7	SysAD34	C8	VccInt
C9	SysAD0	C10	SysADC4	C11	SysADC7	C12	VccInt
C13	SysAD31	C14	SysAD61	C15	VccInt	C16	Do Not Connect
C17	Do Not Connect	C18	VccIO	C19	Vss	C20	Vss
D1	Do not Connect	D2	Vss	D3	Do not Connect	D4	VccIO
D5	VccIO	D6	Do Not Connect	D7	VccInt	D8	VccInt
D9	VccIO	D10	VccInt	D11	VccInt	D12	VccIO
D13	SysAD63	D14	VccInt	D15	SysAD28	D16	VccIO
D17	VccIO	D18	Do Not Connect	D19	Vss	D20	Do Not Connect
E1	SysAD5	E2	Do Not Connect	E3	VccInt	E4	VccIO
E17	VccIO	E18	Do Not Connect	E19	Do Not Connect	E20	SysAD59
F1	Vss	F2	SysAD36	F3	SysAD4	F4	VccInt
F17	VccInt	F18	SysAD27	F19	SysAD58	F20	Vss
G1	SysAD38	G2	SysAD6	G3	SysAD37	G4	VccInt
G17	VccInt	G18	SysAD26	G19	SysAD57	G20	SysAD25
H1	SysAD7	H2	SysAD39	H3	SysAD40	H4	SysAD8
H17	SysAD24	H18	SysAD56	H19	SysAD55	H20	SysAD23
J1	Vss	J2	SysAD9	J3	VccInt	J4	VccIO
J17	VccIO	J18	SysAD54	J19	SysAD22	J20	Vss
K1	SysAD41	K2	SysAD10	K3	SysAD42	K4	SysAD11
K17	SysAD53	K18	SysAD21	K19	SysAD52	K20	SysAD20
L1	SysAD43	L2	SysAD44	L3	SysAD12	L4	VccInt
L17	VccInt	L18	SysAD51	L19	SysAD19	L20	SysAD50
M1	Vss	M2	SysAD13	M3	SysAD45	M4	VccIO
M17	VccIO	M18	SysAD18	M19	SysAD49	M20	Vss
N1	SysAD14	N2	SysAD46	N3	VccInt	N4	SysAD47
N17	VccInt	N18	SysAD48	N19	SysAD16	N20	SysAD17

MIP7365 256 TBGA NUMERICAL PINOUT vs FUNCTION [1,2]

Pin	Function	Pin	Function	Pin	Function	Pin	Function
P1	SysAD15	P2	RspSwap*	P3	PAck*	P4	VccInt
P17	ColdReset*	P18	VccOK	P19	BigEndian	P20	Reset*
R1	Vss	R2	Do Not Connect	R3	JTDI	R4	JTCK
R17	VccInt	R18	ExtRqst*	R19	NMI*	R20	Vss
T1	PRqst*	T2	JTDO	T3	VccIO	T4	JTRST*
T17	VccIO	T18	VccInt	T19	INT9*	T20	INT8*
U1	ModeClock	U2	Vss	U3	JTMS	U4	VccIO
U5	VccIO	U6	ValidIn*	U7	Vss P	U8	VccInt
U9	VccIO	U10	VccInt	U11	VccInt	U12	VccIO
U13	SysCmd7	U14	VccInt	U15	INT3*	U16	VccIO
U17	VccIO	U18	INT6*	U19	Vss	U20	INT7*
V1	Vss	V2	Vss	V3	VccIO	V4	RDType
V5	RdRdy*	V6	VccP	V7	SysClock*	V8	VccInt
V9	Do Not Connect	V10	VREF-In	V11	VccInt	V12	SysCmd3
V13	SysCmd6	V14	VccInt	V15	INT2*	V16	INT5*
V17	INT4*	V18	VccIO	V19	Vss	V20	Vss
W1	Vss	W2	VccIO	W3	Vss	W4	Vss
W5	WRRdy*	W6	Release*	W7	SysClock	W8	VccInt
W9	Do Not Connect	W10	Do Not Connect	W11	SysCmd1	W12	SysCmd2
W13	SysCmd5	W14	SysCmdP	W15	VccInt	W16	INT1*
W17	Vss	W18	Vss	W19	VccIO	W20	Vss
Y1	VccIO	Y2	Vss	Y3	Vss	Y4	ModeIn
Y5	ValidOut*	Y6	Vss	Y7	VccP	Y8	Do Not Connect
Y9	Vss	Y10	Do Not Connect	Y11	SysCmd0	Y12	Vss
Y13	SysCmd4	Y14	SysCmd8	Y15	Vss	Y16	VccJ
Y17	INT0*	Y18	Vss	Y19	Vss	Y20	VccIO

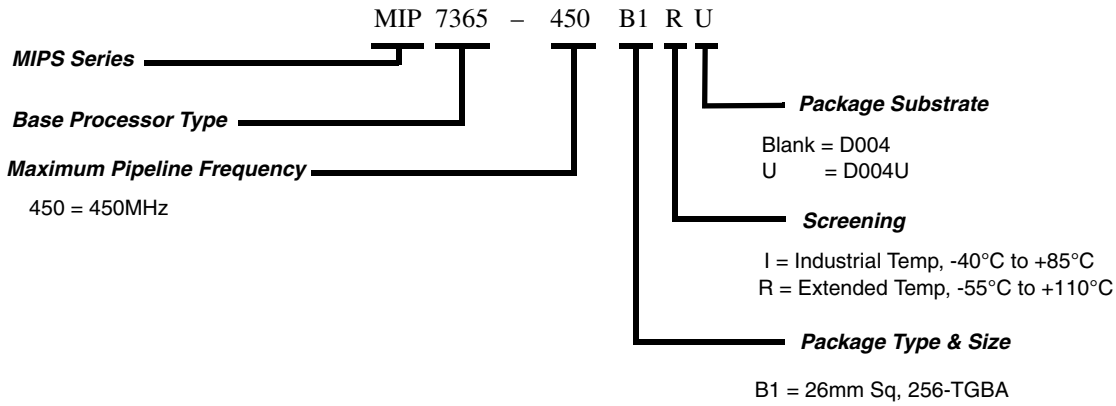
PART NUMBER BREAKDOWN

MIP7365 216-EPad LQFP


MIP 7365 – 450 P R
MIPS Series
Base Processor Type
Maximum Pipeline Frequency
450 = 450MHz
Screening
I = Industrial Temp, -40°C to +85°C
R = Extended Temp, -55°C to +110°C
Package Type & Size
P = 26mm Sq, 216-EPad LQFP

PART NUMBER BREAKDOWN

MIP7365 256 TBGA



SAMPLE ORDERING INFORMATION

PART NUMBER	SCREENING	PIPELINE FREQ (MHZ) Note 2	PACKAGE
MIP7365-450PI 1/	Industrial Temperature Range -40°C to +85°C Testing	450	216-EPad LQFP
MIP7365-450PR 1/	Extended Temperature Range -55°C to +110°C Testing		
MIP7365-450B1I 1/	Industrial Temperature Range -40°C to +85°C Testing	450	256 TBGA
MIP7365-450B1R 1/	Extended Temperature Range -55°C to +110°C Testing		
MIP7365-450B1IU 2/	Industrial Temperature Range -40°C to +85°C Testing		
MIP7365-450B1RU 2/	Extended Temperature Range -55°C to +110°C Testing		

Notes: 1. Substrate D004
2. Substrate D004U

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